(When) Will FPGAs Kill ASICs?

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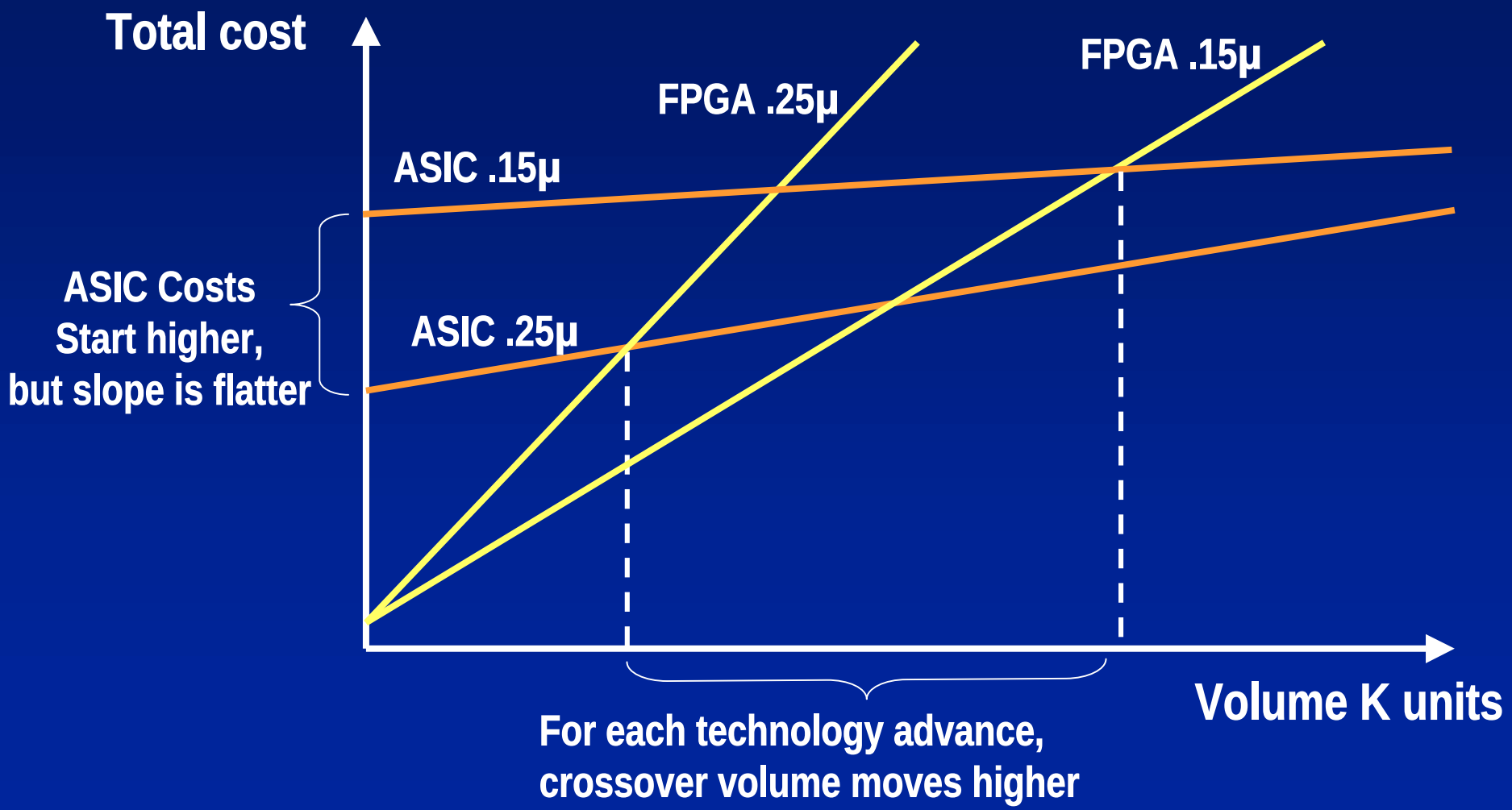
DAC-2001

FPGAs vs. ASICs

- Cost – the real story.
- Time to market
- Why choose ASICs?
- Where are FPGAs going?

Unit Cost Analysis



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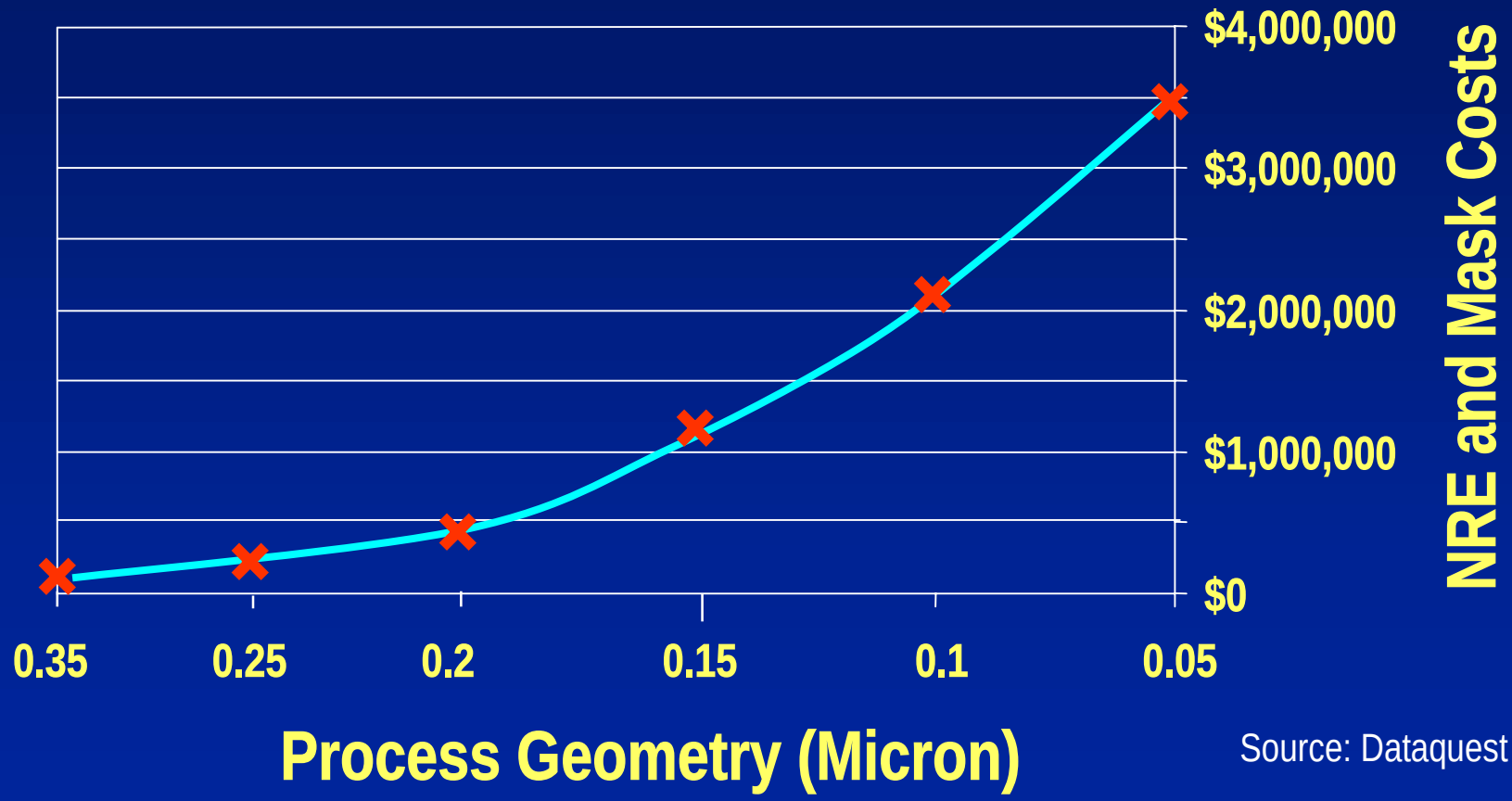
Cost: The exploding ASIC NRE



Source: Dataquest

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Time to market is critical

Missing the market window will wipe out all savings from development and production

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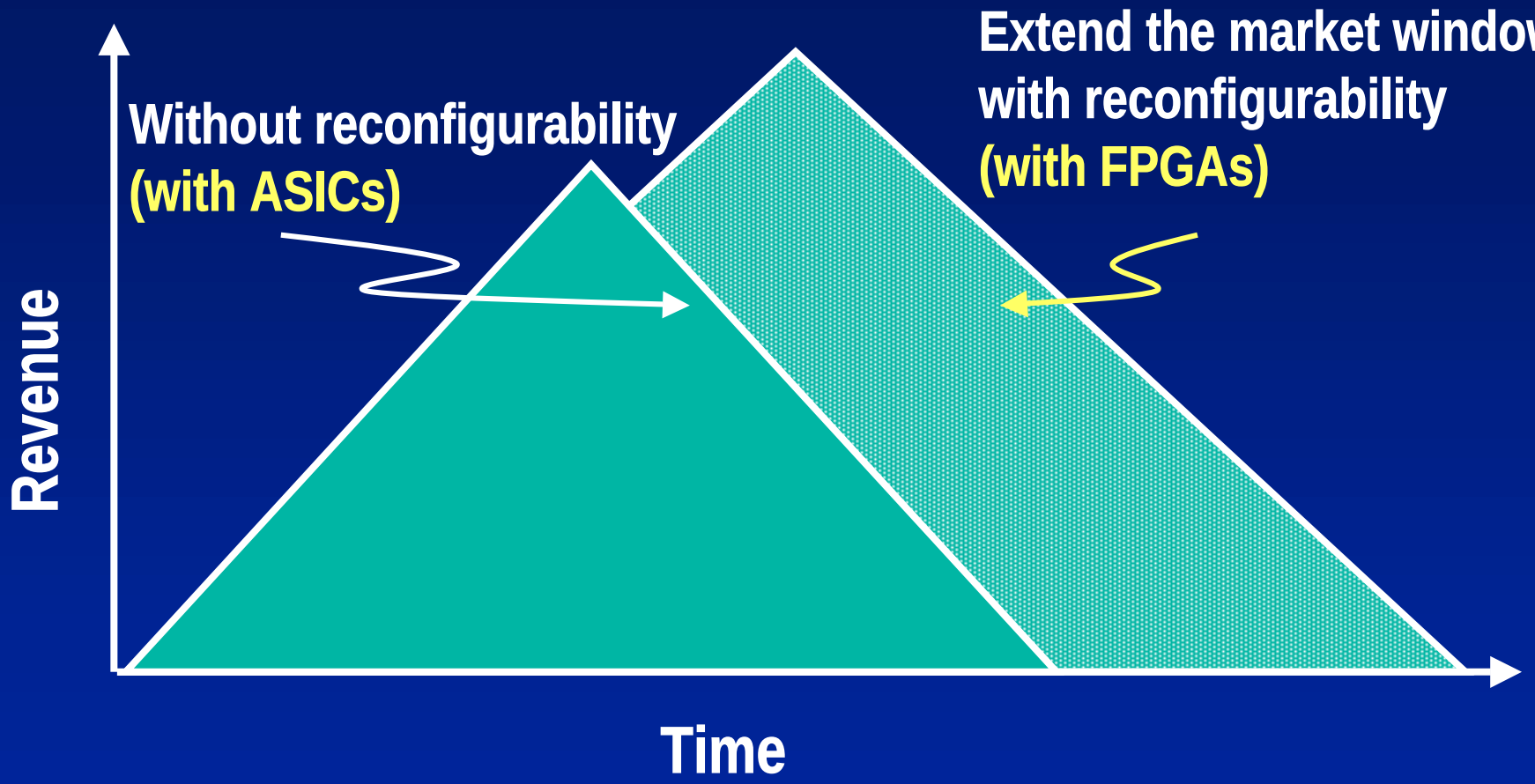
COST: System Reconfigurability



Lack of reconfigurability is a huge opportunity cost of ASICs

FPGAs offer flexible life cycle management

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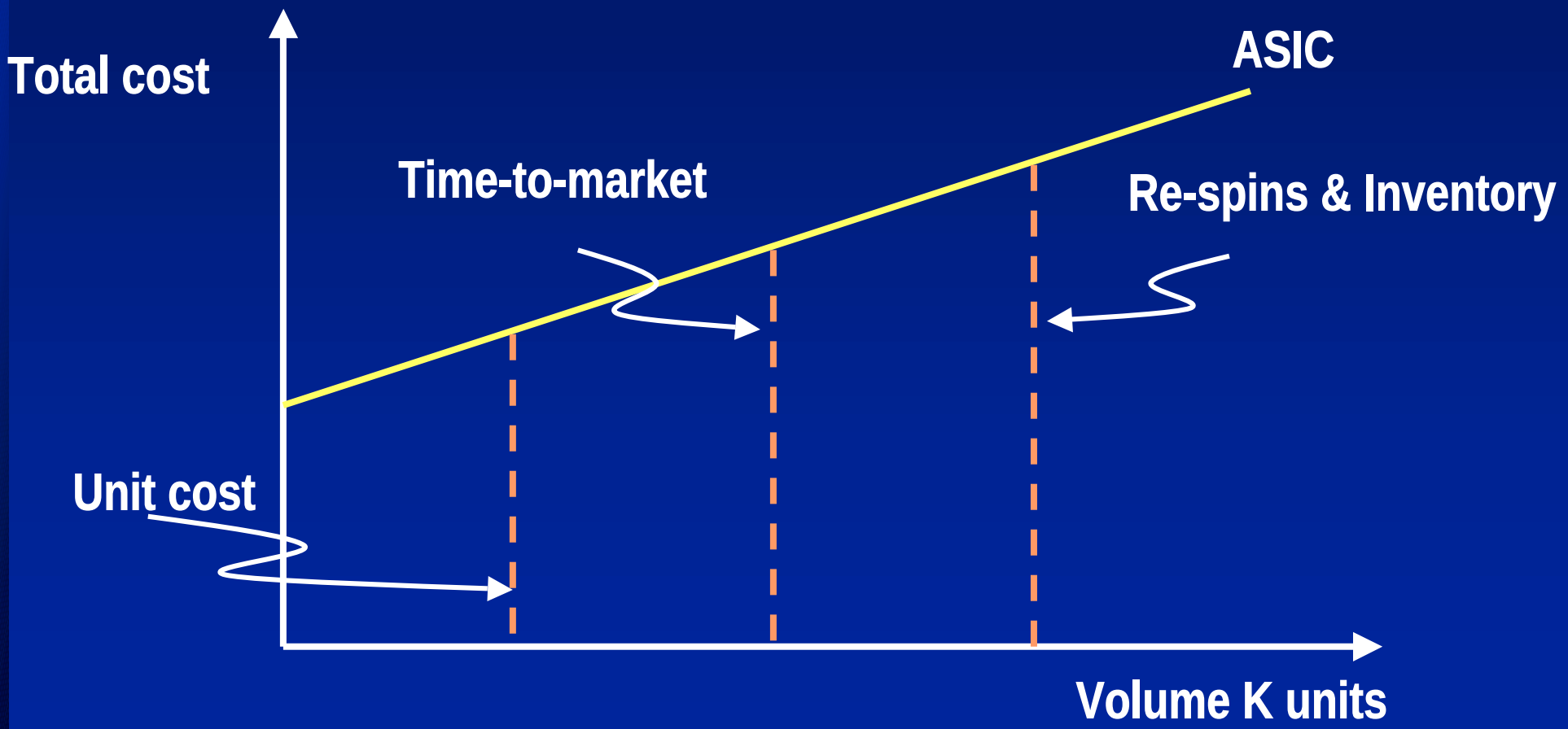
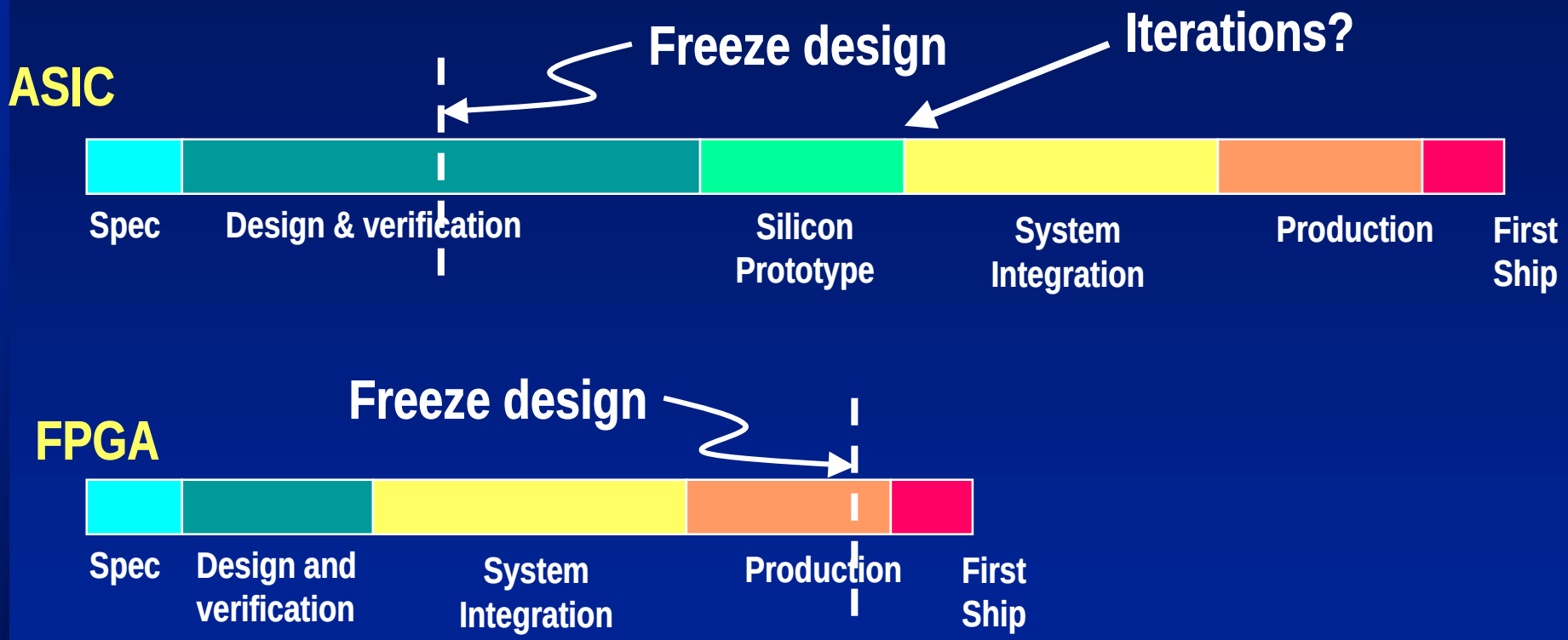
Breakeven Cost: Just the facts



Time To Market: Design Cycle



- ASIC Methodology is very unforgiving
- FPGA flexibility allows late design changes

Designing with ASICs

DSM
Effects

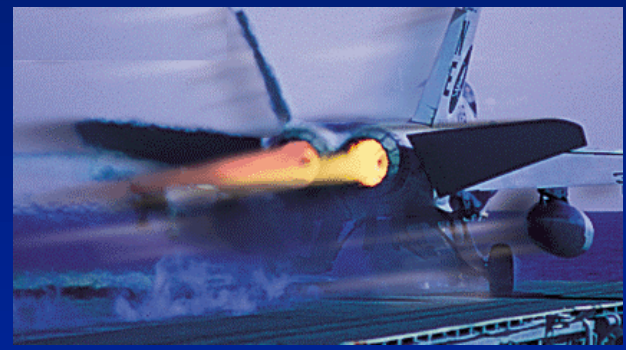
Verification

Process
issues

Timing Closure is a very serious problem in DSM

Designing with FPGAs

Verification
is much simpler



Super fast compile times
~1M gates in < 1hr

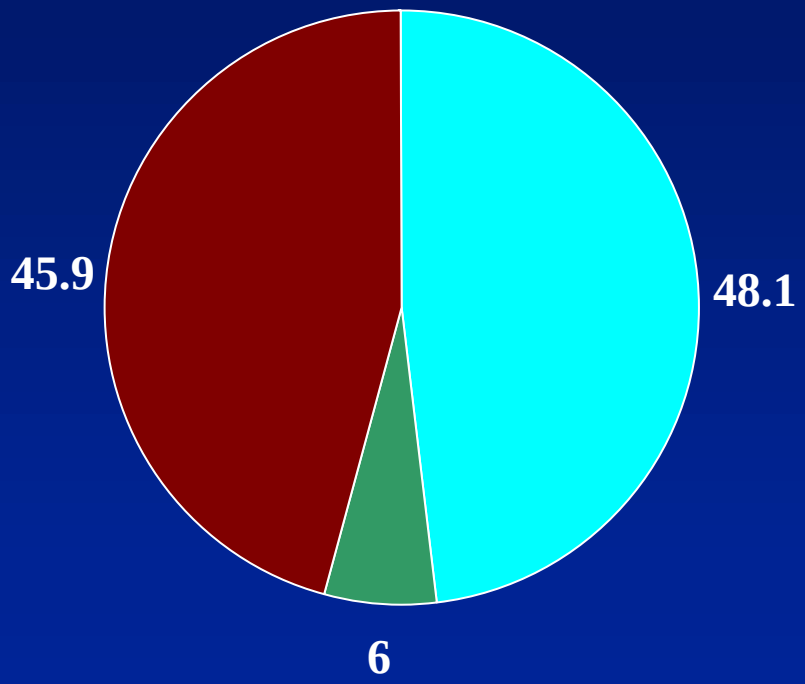
Timing Closure is a much simpler problem in FPGAs

Why do people design ASICs?

- Cost/Volume
- Performance
- Density
- IP Libraries

Volume requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries



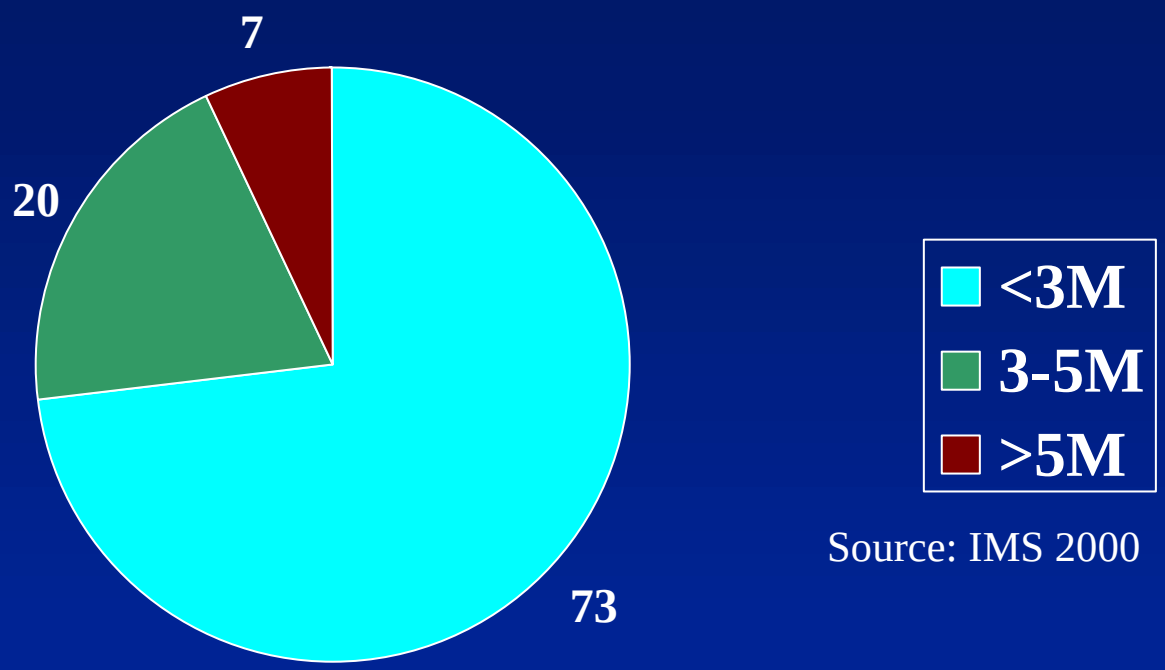
- <100K
- 100-250K
- >250K

Source: IMS 2000

>50% of market is available today for FPGAs

Gate count requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

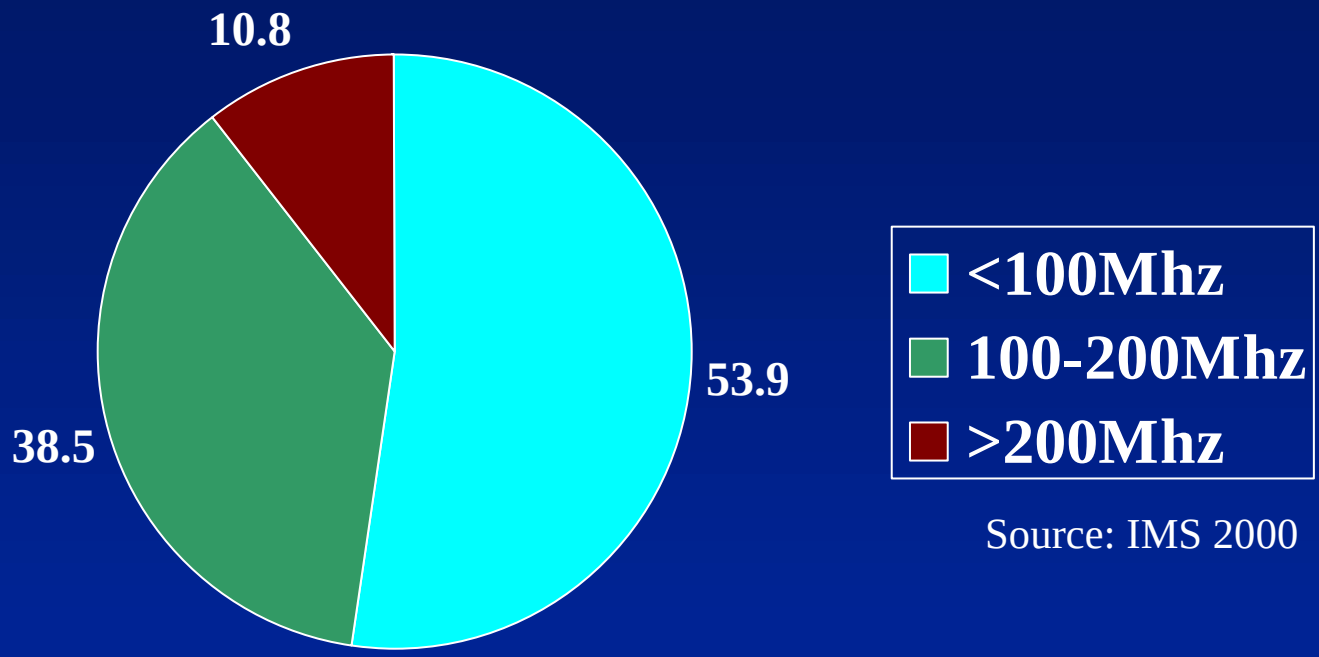


Source: IMS 2000

FPGAs can address very large part of the ASIC market today

Performance requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

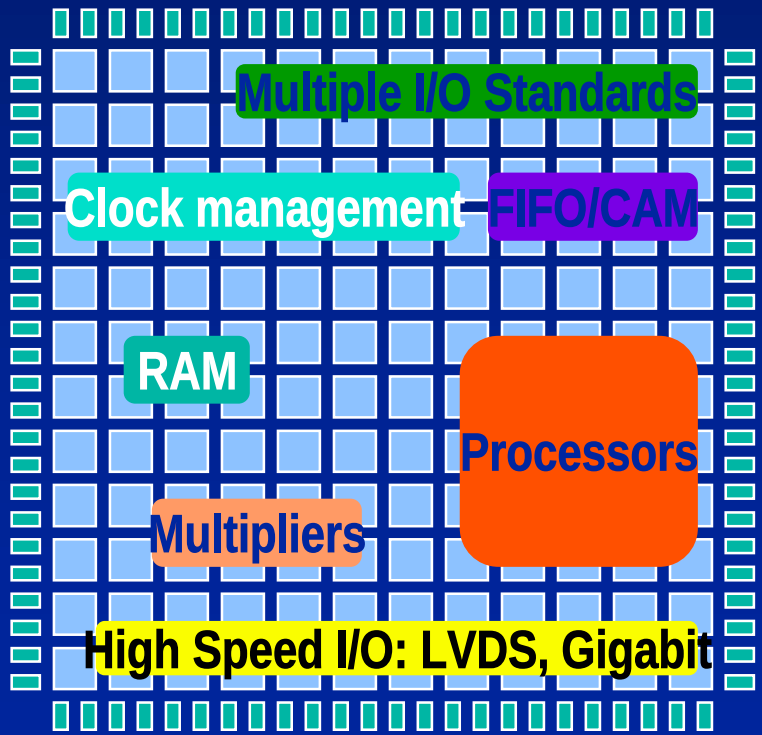


Source: IMS 2000

FPGAs can address very large part of the ASIC market today

IP in FPGAs

- Cost
- Density
- Performance
- IP Libraries



5 Years ago FPGAs were only gates and routing
~25000 gates

Today, there are several system-level features.
~10,000,000 gates

The trend to add more IP in FPGAs continues

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The Question is …

- The question is not if FPGAs will kill ASICs
  - Everyone understands the advantages of programmability
- The real question is “How can I get programmability in my system?”
- More IP on an FPGA or Progammability on an ASIC?

What is the future? You decide…

	More IP on FPGA	More Prog. On ASIC
Time-to-market	Verification remains simple Timing closure is easier	Verification remains a problem Timing closure remains an issue
Cost	NRE is non-existent Extensive reconfigurability	NRE not reduced Very limited reconfigurability
Design methodology/ Software	Simple methodology Ease of use Extremely fast SW runtimes	Still a complex methodology Ease of use is still lacking